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### (54) SENSE AMPLIFIER WITH INTEGRATING CAPACITOR AND METHODS OF OPERATION

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### (57) ABSTRACT

A non-volatile memory is described that includes a sense amplifier that maintains a bit line voltage and output of the sense amplifier at a substantially constant voltage during read operations. During a preset phase, an output of the sense amplifier that is coupled to a selected bit line is grounded. At least one capacitor is precharged during the preset phase. During a sense phase, the sense amplifier output is disconnected from ground while the memory array is biased for reading a selected memory cell. A resulting cell current is integrated by the at least one capacitor. The integrated cell current discharges a sense node from the precharge level to an accurate voltage level based on the resulting cell current.

